WHAT IS CLAIMED IS:

1. A chip package structure, at least comprising:

a carrier having a surface, a power pad and a ground pad, said surface having a die bonding area, said power pad and said ground pad being on said surface, said power pad and said ground pad being disposed outside said die bonding area;

a die having an active surface and a backside corresponding to said active surface, said backside being attached to said die bonding area on said surface of said carrier, said die having a plurality of die pads on said active surface;

at least a passive component disposed between said power pad and said ground pad, said passive component having at least two electrodes connected to said power pad and said ground pad respectively; and

at least a first conducting wire having two ends connected to one of said plurality of die pads and one of said electrodes respectively.

2. The chip package structure of claim 1, further comprising a dielectric material covering said die, said passive component, and said first conducting wire.

3. The chip package structure of claim 1, wherein said carrier comprises a signal pad, said signal pad being disposed outside said die bonding area and farther from said die bonding area than said power pad and said ground pad.

4. The chip package structure of claim 3, further comprising at least a second conducting wire having two ends connected to another one of said plurality of die pads and said signal pad respectively, said second conducting wire crossing over said passive component.

5. The chip package structure of claim 4, further comprising a dielectric material covering said die, said passive component, said first conducting wire, and said

second conducting wire.

6. The chip package structure of claim 1, wherein the surface of said electrodes comprises a metal layer, said metal layer at least including Ni, Au, or Ni/Au alloy.

7. The chip package structure of claim 1, wherein said passive component is selected from one of an inductor and a capacitor.

8. The chip package structure of claim 1, wherein said carrier is a package substrate.

9. A wire bonding package structure for electrically connecting a die to a carrier, said carrier having a surface and a die bonding area on said surface, said die having an active surface and a backside corresponding to said active surface, said backside of said die being attached to die bonding area, said wire bonding package structure at least comprising:

a power pad on said surface of said carrier;

a ground pad on said surface of said carrier;

a signal pad on said surface of said carrier, said power pad, said ground pad and said signal pad being disposed outside said die bonding area, wherein said signal pad being farther from said die bonding area than said power pad and said ground pad;

a passive component disposed between said power pad and said ground pad, said passive component having at least two electrodes connected to said power pad and said ground pad respectively;

a plurality of die pads on said active surface of said die;

a first conducting wire having two ends connected to one of said die pads and one of said electrodes respectively; and

a second conducting wire having two ends connected to another one of said die

pads and said signal pad respectively, wherein said second conducting wire crossing over said passive component.

10. The wire bonding package structure of claim 9, wherein the surface of said electrodes comprises a metal layer, said metal layer at least including Ni, Au, or Ni/Au alloy.

11. The wire bonding package structure of claim 9, wherein said passive component is selected from one of an inductor and a capacitor.

12. The wire bonding package structure of claim 9, further comprising a dielectric material covering said die, said passive component, said first conducting wire, and said second conducting wire.

13. The wire bonding package structure of claim 9, wherein said carrier is a package substrate.